are patterned and cut with the use of a fifth mask. Five hundred angstroms of Cr, 2000 angstroms of Ni and 5000 angstroms of Au are deposited, patterned and lifted off for pad and solder frame metal **33** in FIG. **4***j*. Passivated leadouts **40** in first metal **26** or second metal **27** pass under the seal ring metal **33** in FIG. **4***j*. Plasma etched pump-out port vias **11** are patterned and cut on layers **23***b* and **23***a* of the back of wafer **13** in FIG. **4***k*. There is a KOH etch of the back side of wafer **13** through 90 percent of wafer **13** for port **11** in FIG. **4***l*. Port **11** is completed with an etch through via **32** to the front of wafer **13** as shown in FIG. **4***m*.

Top cap wafer **14**, like detector wafer **13**, is fabricated with films compatible with 300 degree C. bakes and low outgassing. Wafer **14** acts as the window for infrared devices **17**. An additional constraint is that wafer **14** is made from low oxygen silicon (i.e., float zone silicon) to minimize the SiO_2 absorption peak in the 8–14 micron wavelength window. Top cap wafer **14** is coated with an anti-reflection coating **34**. Wafer **14** has a solder adhesion metal and solder ring **15** which matches detector wafer **13**, a border **18** forming chamber **16** above detectors **17**, and holes **35** through wafer **14** to access the wire bond pads on detector wafer **13**.

FIGS. **5***a* through **5***f* illustrate steps of fabrication for top cap **14**. The starting material is a double polished silicon wafer **14** grown by float zone for minimum oxygen content. 1.8 micron layers of thermally grown SiO_2 **36***a* and **37***a* in FIG. **5***a* are covered by 0.3 microns of LPCVD Si_3N_4 layers **36***b* and **37***b* to mask the KOH etching. Pattern and cut via **35** by plasma etching on outside layers **36***a* and **36***b* and recess **16** on inside layer **37***b* of Si_3N_4 in FIG. **5***b*. The wafer **14** is then put in a fixture to allow etching of the outside surface **35** and **36***b* while protecting the inside **16** and **37***b* to KOH etch wafer **14** through hole **35** to 90 percent of the way through top cap wafer **14**, as shown in FIG. **5***c*. Wafer **14** is removed from the etching fixture and hole **16** is cleared of remaining SiO2 layer **37***a* in FIG. **5***d* by buffered oxide etch. Hole **35** is further etched through wafer **14** to layer **37***a* to complete bond pad hole **35**. Also, FIG. **5***d* shows the etching that creates recess **16** on the inside of wafer **14**. Nitride and oxide mask layers **36***a*, **36***b*, **37***a* and **37***b* are stripped from wafer **14**. Antireflective coating **38** is applied to wafer **14**. A solder ring pattern is applied to the inside surface encircling recess **16**, by using a laminated Riston process for lift-off. Five hundred angstroms of Ti, 2000 angstroms of Ni and 500 angstroms of Au of adhesion metals **39** are deposited in an E-beam evaporator. A five micron layer **40** of InPb (10:90) solder is deposited onto adhesion metals **39** in the thermal evaporator. The Riston mask is lifted off and the field SiO_2 in BOE etched off resulting in solder ring **18** in FIG. **5***f*.

Bonding and sealing detector wafer **13** and top cap wafer **14** are done with clean surfaces. Bonding surfaces of wafers **13** and **14** are sputter cleaned just prior to doing the wafer bond. The following sequence of events indicate how to align, bond and seal the wafer pair **13** and **14** of FIGS. **6***a*, **6***b* and **6***c*. To begin, the Au solder ring surface **33** of detector wafer **13** is sputter cleaned. The InPb surface of ring **18** of top cap wafer **14** is oxygen plasma cleaned. Wafers **13** and **14** of FIG. **6***a* are aligned in a bonding cassette using 0.002 inch spacers between the wafers. The aligned wafer pair is put in a vacuum press which is pumped to a good vacuum with a turbo pump. Wafers **13** and **14** are pressed together in FIG. **6***b*, with about 400 pounds of pressure. The temperature of the wafers is ramped up to 300 degrees C., which takes about one hour. Then wafers **13** and **14** are held at this achieved temperature and pressure for five minutes. Then wafers **13** and **14** are cooled down to room temperature, and the vacuum chamber is vented.

Bonded wafer pair **13** and **14** is put into an E-beam evaporation system for sputter cleaning of the pump-out port **11** surfaces, followed by adhesion layers of 500 angstroms of Ti, 1000 angstroms of Ni and 500 angstroms of Au. Wafer pair **13** and **14** is put into a thermal evaporator system; and a bake out of the wafer pair at 250 degrees C. is preferred for four hours under a vacuum. The wafer pair **13** and **14** is cooled down but the environment about the wafer pair is kept at the desired vacuum. Twenty microns of InPb (50:50) **12** is deposited onto the backside of detector wafer **13** to plug port **11** in FIG. **6***c*, to seal vacuum chamber **16** of wafer pair **13** and **14**. On the wafer **20** scale, a plurality of ports **11** in a plurality of chips are plugged. Then wafers **13** and **14**, combined as wafer **20**, may be removed from the vacuum environment. Wafer **20** may be cut into individual chips **10**, each having its own sealed chamber **16** enclosing detectors **17**.

Further variations on this theme include top cap wafer **14** composed of Germanium for better IR transmission or ZnSe for broadband transmission (i.e., visible and IR)or other optical window materials for application specific optical bandpass behavior. Top cap wafer **14** may have integrated components built in or on the surface in addition to those on the detector wafer **13**. Detector wafer **13** having a diaphragm pressure sensor integrated into it, the sealed chamber then forms a vacuum pressure reference. Detector wafer **13** may have infrared bolometer arrays with readout electronics integrated into the wafer. Detector wafer **13** may have moving parts to be sealed in a chamber for other functional purposes. The bonded wafer pair **13** and **14** in FIG. **6***c* may be hermetically sealed with a controlled residual pressure of a specific gas type for optimal thermal, mechanical or other properties rather than simply evacuated for the devices within the chamber.

We claim:

1. A method for making a wafer-pair having deposited layer plugged sealed chambers, comprising:

growing a thermal layer on a first side of a first silicon wafer;

depositing a nitride layer on the thermal layer;

depositing, patterning and removing portions of first metal layer on the nitride layer for a plurality of devices;

depositing, patterning and removing portions of a second metal layer on the nitride and first metal layers for the plurality of devices;

patterning and removing material from the first silicon wafer and layers on the first side of the first silicon wafer and from a second side of the first silicon wafer to make a plurality of pump-out ports through the first silicon wafer and layers on the first silicon wafer;

masking and removing material from a first side of a second silicon wafer to form a plurality of recesses in the first side of the second silicon wafer;

forming a sealing ring on the first side of the second silicon wafer around each of the plurality of recesses; and

positioning the first side of the first silicon wafer next to the first side of the second silicon wafer; and

wherein:

each sealing ring is in contact with at least one of the layers on the first side of the first silicon wafer;

each recess of the plurality of recesses results in a chamber containing at least one device of the plurality of devices;

each sealing ring encloses at least one pump-out port of the plurality of pump-out ports; and

the first and second silicon wafers are effectively a bonded together set of wafers.

2. The method of claim 1, further comprising:

placing the set of wafers in an environment of a vacuum wherein a vacuum occurs in each chamber via the at least one pump-out port; and

depositing a layer of material on the second side of the first silicon wafer and the plurality of pump-out ports on the second side of the first silicon wafer, wherein each chamber is sealed from the environment.

3. The method of claim 2, further comprising baking out the set of wafers prior to depositing the layer of material on the second side of the first wafer and the plurality of pump-out ports on the second side of the first silicon wafer.

4. The method of claim 3, further comprising coating the second wafer with antireflection material.

5. The method of claim 4, wherein the second silicon wafer is made from low oxygen silicon or float zone silicon to minimize an absorption peak in an 8–14 micron wavelength region of light going through the second silicon wafer to the plurality of devices.

6. The method of claim 5, wherein the set of wafers is cut into a plurality of chips wherein each chip has one or more sealed chambers.

7. The method of claim 6, wherein the plurality of devices comprise thermoelectric detectors.

8. The method of claim 6, wherein the plurality of devices comprise bolometers.

9. A method for making a wafer-pair having at least one deposited layer plugged sealed chamber, comprising:

growing a first thermal layer on a first side of a first silicon wafer;

depositing a nitride layer on the first thermal layer;

depositing and patterning a first metal layer on the nitride layer for at least one device;

depositing and patterning a second metal layer on the nitride layer and the first metal layer for the at least one device;

patterning and removing material from the first silicon wafer and layers on the first side of the first silicon wafer and from a second side of the first silicon wafer to make a pump-out port through the first silicon wafer and the layers on the first silicon wafer;

masking and removing material from a first side of a second silicon wafer, to form a recess in the first side of the second silicon wafer;

forming a sealing ring on the first side of the second silicon wafer around the recess; and

positioning the first side of the first silicon wafer next to the first side of the second silicon wafer; and

wherein:

the sealing ring is in contact with at least one of the layers on the first side of the first silicon layer;

the at least one device is within the recess resulting in a chamber containing the at least one device;

the pump-out port is within the sealing ring; and

the first and second silicon wafers are effectively a bonded together set of wafers.

10. The method of claim 9, further comprising:

placing the bonded together set of wafers in an environment of a vacuum wherein a vacuum occurs in the chamber via the pump-out port; and

depositing a layer of material on the second side of the first silicon wafer and the pump-out port on the second side of the first silicon wafer, wherein the chamber is sealed from the environment.

11. The method of claim 10, further comprising baking out the bonded together set of wafers prior to depositing the layer of material on the second side of the first wafer and the pump-out port on the second side of the first silicon wafer.

12. The method of claim 11, wherein the at least one device is a detector.

13. The method of claim 12, further comprising coating the second silicon wafer with antireflection material.

14. The method of claim 11, wherein the second silicon wafer is made from low oxygen silicon or float zone silicon to minimize an absorption peak in an 8–14 micron wavelength region of light going through the second silicon wafer to the at least one device.

15. The method of claim 14, wherein the at least one device is a thermoelectric detector.

16. The method of claim 14, wherein the at least one device is a bolometer.

17. The method of claim 11, wherein the at least one device is an emitter.

18. A method for making a wafer-pair having at least one deposited layer plugged sealed chamber, comprising:

growing a first layer of thermal SiO_2 on a first side of a first silicon wafer;

depositing a first layer of Si_3N_4 on the first layer of thermal SiO_2;

growing a second layer of thermal SiO_2 on a second side of the first silicon wafer;

depositing a second layer of Si_3N_4 on the second layer of thermal SiO_2;

depositing a layer of a first metal on the second layer of Si_3N_4;

patterning the layer of the first metal;

depositing a layer of a second metal on the layer of the first metal;

patterning the layer of the second metal;

depositing a third layer of Si_3N_4 on the layers of the first and second metals;

etching at least one via through the third layer of Si_3N_4, the layers of the second and first metals, the second layer of Si_3N_4 and the second layer of thermal SiO_2;

etching a pump-out port through the first layer of SiO_2 and a first portion of the silicon wafer proximate to the at least one via;

etching within the at least one via through a second portion of the silicon wafer to the pump-out port;

growing a third layer of thermal SiO_2 on a first side of a second silicon wafer and a fourth layer of

thermal SiO_2 on a second side of the second silicon wafer;

growing a fourth layer of Si_3N_4 on the third layer of thermal SiO_2 and a fifth layer of Si_3N_4 on the fourth layer of SiO_2;

patterning and cutting the fourth layer Si_3N_4 and the third layer of thermal SiO_2 for a bond pad area;

etching a first portion of the second silicon wafer through the fourth Si_3N_4 layer and third SiO_2 layer for the bond pad area;

patterning and cutting the fifth layer of Si_3N_4 and fourth layer of thermal SiO_2 for a recess area;

etching a second portion from the second side of the second silicon wafer to form a recess;

applying an optical coating to the second silicon wafer to substantially reduce reflections;

applying a solder ring proximate to a perimeter of the recess, on the second side of the second silicon wafer;

aligning the first silicon wafer with the second silicon wafer, having the first side of the first silicon wafer and the second side of the second silicon wafer face each other;

putting the first and second silicon wafers in a vacuum;

pressing the first and second silicon wafers together with a pressure;

ramping the temperature of the silicon wafers up to a high temperature;

increasing the pressure of the first and second silicon wafers against each other to bond the silicon wafers to each other;

baking out the first and second silicon wafers;

cooling down the first and second silicon wafers under a maintained vacuum;

depositing a layer of a metal on the second side of the second silicon wafer to plug the pump-out port to seal the recess with a vacuum; and

removing the bonded first and second silicon wafers from the vacuum.

19. A method for making a wafer-pair having deposited layer plugged sealed chambers, comprising:

growing a thermal layer on a first side of a first silicon wafer;

patterning and removing material from the first silicon wafer and layers on the first side of the first silicon wafer and from a second side of the first silicon wafer to make a plurality of pump-out ports through the first silicon wafer and layers on the first silicon wafer;

masking and removing material from a first side of a second silicon wafer to form a plurality of recesses in the first side of the second silicon wafer;

forming a sealing ring on the first side of the second silicon wafer around each of the plurality of recesses; and

positioning the first side of the first silicon wafer next to the first side of the second silicon wafer; and

wherein:

each sealing ring is in contact with at least one of the layers on the first side of the first silicon layer;

each recess of the plurality of recesses results in a chamber;

each sealing ring encloses at least one pump-out port of the plurality of pump-out ports; and

the first and second silicon wafers are effectively a bonded together set of wafers.

20. The method of claim **19**, further comprising:

placing the set of wafers in an environment of a vacuum wherein a vacuum occurs in each chamber via a pump-out port; and

depositing a layer of material on the second side of the first silicon wafer and the plurality of pump-out out ports on the second side of the first silicon wafer, wherein each chamber is sealed from the environment.

21. The method of claim **20**, further comprising baking out the set of wafers prior to depositing the layer of material on the second side of the first wafer and the plurality of pump-out ports on the second side of the first silicon wafer.

22. The method of claim **21**, wherein the set of wafers is cut into a plurality of chips wherein each chip has one or more sealed chambers.

23. The method of claim **22**, wherein the one or more sealed chambers contains one or more devices.

24. The method of claim **19**, further comprising:

placing the set of wafers in an environment of a gas wherein the gas enters each chamber via a pump-out port; and

depositing a layer of material on the second side of the first silicon wafer and the plurality of pump-out ports on the second side of the first silicon wafer, wherein each chamber is sealed from an ambient environment.

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